100G QSFP28 10km PSM4 Transceivers

RQ-100G-PSM4

Product Description

The RQ-100G-PSM4 QSFP28 optical transceiver is intended for up to 10km reach service with four-lane 25.78125G data rate. It is based on 3.3V DC power supply and operates in the commercial temperature range. It is compliant with QSFP MSA 、SFF-8436 、SFF-8636 and PSM4 MSA. Digital diagnostic functions are available via I2C interface， and the control functions can be achieved by LVTTL interfaces on the host， mainly including Module Select(ModSelL)、 Module Reset(ResetL)、 Low Power Mode(LPMode). The transceiver incorporates a four-laser array which is usually DFB 、four-PIN diode array 、a high performance CDR integrated four drivers and TIAs IC separately. The differential AC coupled Tx and Rx data interfaces are CML compatible.

Applications

- 100G BASE Ethernet
- Infiniband EDR interconnects
- Enterprise networking

Features

- MPO12 optical interface
- Maximum link length up to 10km
- Up to 25.78125Gb/s data links per lane
- +3.3 V power supply
- QSFP MSA compliant package
- Hot Pluggable
- High performance singal mode DML transmitter
- High sensitivity PIN/TIA optical receiver
- Single Mode operation
- BER < 5E-5@-12.5dBm（OMA）
- Built-in CDR
- Case Operating temperature : 0 to 70ºC
- Data and Control Interfaces
- Tx Data CML/AC Coupled
- Rx Data CML/AC Coupled
- ModSelL LVTTL
- ResetL LVTTL
- ModPrsL LVTTL
- LPMode LVTTL
- 2-wire I2C communication bus
- RoHS 6 compliance

Ordering Code

Ordering Information	
Part Number	**Case Operating Temperature**
RQ-100G-PSM4	**100G QSFP28 10km PSM4 0 to 70 ºC**

Absolute maximum parameters

Absolute Maximum Ratings (EXCEEDING THESE RATINGS MAY CAUSE IRREVERSIBLE DAMAGE TO THE DEVICE)					
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Notes**
Storage Temperature	T_{stg}	-40	+95	ºC	Exceeding the absolute maximum ratings may cause irreversible damage to the device. The device is not intended to be operated under the condition of simultaneous absolute maximum ratings, which may cause irreversible damage to the device.
Case Operating Temperature (Commercial)	T_O	0	+70	ºC	
Relative Humidity - Storage	R_{HS}	0	95	%	
Relative Humidity - Operating	R_{HO}	0	85	%	
Supply Voltage	VCC	-0.3	3.6	V	

Operating conditions

Recommended Operating Conditions						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Case Operating Temperature	T_{case}	0	-	+70	ºC	
DC Supply Voltage	VCC	3.135	-	3.465	V	
Module Supply Current	I_{IN}	-	-	1000	mA	

Electrical Characteristics

Transmitter Electrical Characteristics						
Parameter	**Symbol**	**Mi**	**Typ**	**Max**	**Units**	**Notes**
Differential Data input Swing	V_{IN}	180	-	900	mV	
Tx Differential Input Impendence	Z_{in}	90	100	110	Ω	
Tx Differential Output Impendence	Z_{out}	45	50	55	Ω	

ResetL Disable Voltage	V_r	2.0	-	Vcc+0.3	V	
ResetL Enable Voltage	V_{rEN}	0	-	0.8	V	
ModSelL Disable Voltage	V_m	2.0	-	Vcc+0.3	V	
ModSelL Enable Voltage	V_{mEN}	0	-	0.8	V	

Receiver Electrical Characteristics						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Differential Data Output Swing	V_{OUT}	180	-	900	mV	
Rx Differential Output Impendence	Z_{OUT}	90	100	110	Ω	
IntL Assert Voltage	V_{Int}	VCC-0.5	-	VCC+0.3	V	
IntL De-assert Voltage	VD_{Int}	0	-	+0.4	V	

Optical Specification

Transmitter Optical Specification						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Signal Rate|Each Lane			25.78125 ±100ppm		Gbps	
Lane Wavelength	L0	1295	1310	1325	nm	
	L1	1295	1310	1325	nm	
	L2	1295	1310	1325	nm	
	L3	1295	1310	1325	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	P_{tol}			8.0	dBm	
Average Launch Power|Each Lane	P_{avg}	-9.4		2.0	dBm	
Optical Modulation Amplitude|Each Lane	OMA			2.2	dBm	1
Transmitter and dispersion penalty|Each Lane	TDP			2.9	dB	
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3		{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}				2
Average launch power of OFF transmitter|Each Lane				-30	dBm	
Extinction Ratio	ER	3.5			dB	
Spectral Width|20dB				1	nm	
Transmitter Reflectance				-12	dB	
Optical return loss tolerance				20	dB	

Note:

1. Even if the TDP < 1 dB, the OMA min must exceed the minimum value specified here.
2. Hit ratio of 5e-5, per IEEE.

Receiver Optical Specification						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Signal Speed Per Lane			25.78125 ±100ppm		Gbps	
Lane Wavelength	L0	1295	1310	1325	nm	
	L1	1295	1310	1325	nm	
	L2	1295	1310	1325	nm	
	L3	1295	1310	1325	nm	
Damage threshold|Each Lane	THd			3.0	dBm	1
Average Receive Power|Each Lane		-12.66		2.0	dBm	
Receiver reflectance				-26	dB	
Sensitivity OMA|Each Lane[1]	Sen			-12.5	dBm	2
Stressed Receiver Sensitivity (OMA), each Lane				-8.8	dBm	
LOS Assert	LOSA		-15.5			
LOS Deassert	LOSD		-13.5			
LOS Hysteresis	LOSH	0.5		3		
Vertical Eye Closure Penalty	VECP	1.9			dB	3
Stressed Eye J2 Jitter	J2		0.27		UI	
Stressed Eye J4 Jitter	J4		0.39		UI	

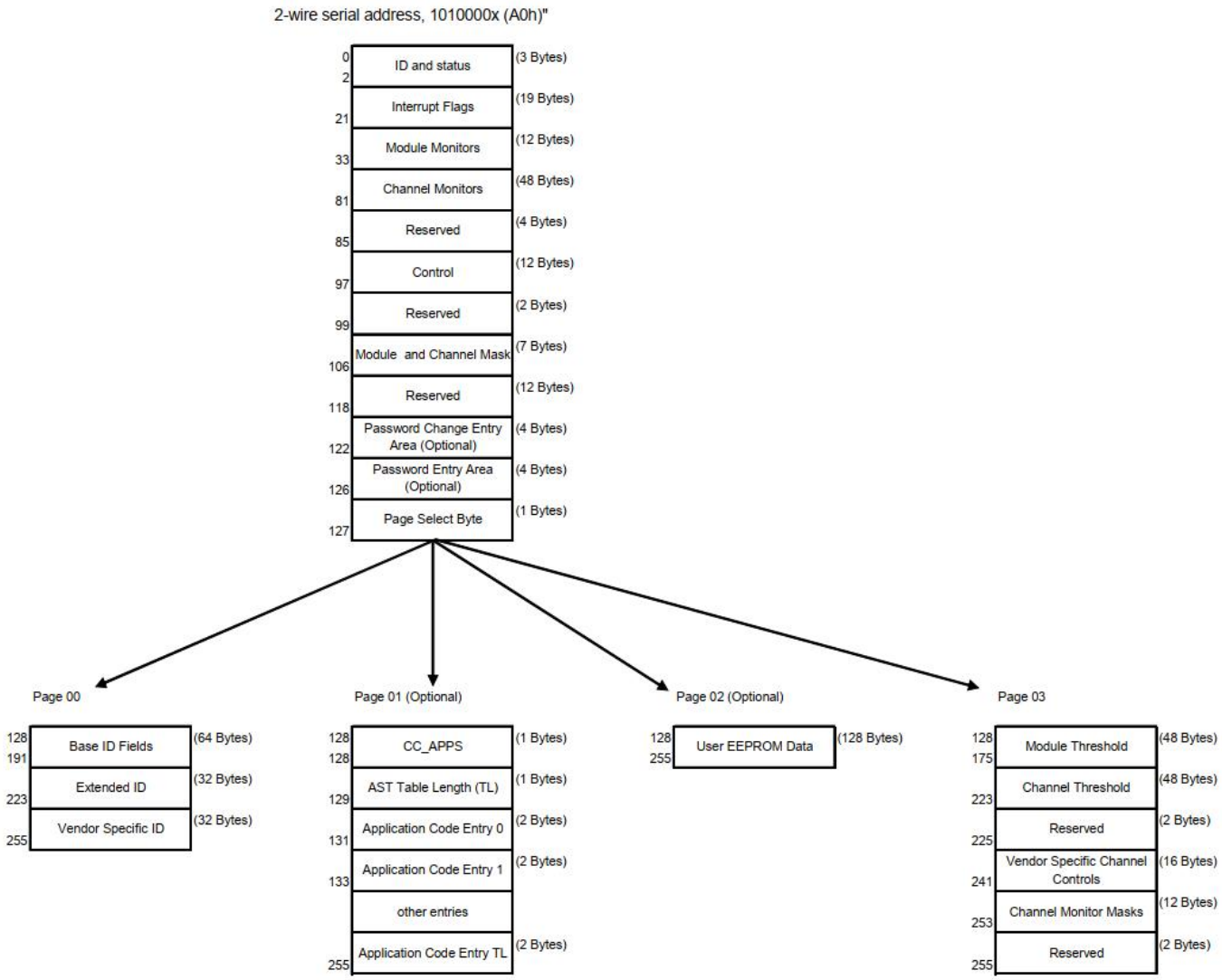
Note:

1. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
2. Measured with conformance test signal at receiver input for BER = 5e-5 BER.
3. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver

Digital diagnosti

Monitoring Interface				
Parameter	Symbol	Spec	Units	Condition/Notes
Temperature	Te	+/-3	°C	
Voltage	VCC	+/-5%	V	
IBias	BIAS	+/-10%	mA	
Rx power	Rx-pwr	+/-2	dBm	
Tx power	Tx-pwr	+/-2	dBm	

Memery Map



I2C Memory Map (A0 Lower Page 00h, Unlisted Fields are Blank / Empty)				
I2C Addr	**Size**	**Name**	**Description**	**Values (hex)**
0	1	Identifier	Identifier(QSFP28)	11
1	2	Status	Revision Compliance	08
2			Status(Flat_mem、IntL、Data_Not_Ready 标志)	
3	19	Interrupt Flags	L-Tx/RX LOS, channel 1~4	
4			L-Tx Adapt EQ Fault, channel 1~4 L-TX Fault, channel 1~4	
5			L-Tx/RX LOL, channel 1~4	
6			L-Temp High/Low Alarm/Warning Initialization complete flag	
7			L-VCC High/Low Alarm/Warning	
8			Vendor Specific	
9			L-Rx Power High/Low Alarm/Warning, channel 1~2	
10			L-RxPower High/Low Alarm/Warning, channel 3~4	
11			L-Tx Bias High/Low Alarm/Warning, channel 1~2	
12			L-Tx Bias High/Low Alarm/Warning, channel 3~4	
13			L-Tx Power High/Low Alarm/Warning, channel 1~2	
14			L-Tx Power High/Low Alarm/Warning, channel 3~4	
15~18			Reserved	
19~21			Vendor Specific	
22	12	Free Side Device Monitors	Internally measured temperature (MSB)	
23			Internally measured temperature (LSB)	
24~25			Reserved	
26			Internally measured supply voltage (MSB)	
27			Internally measured supply voltage (LSB)	
28~29			Reserved	
30~33			Vendor Specific	
34	48	Channel Monitoring	Internally measured RX input power, channel 1 (MSB)	
35			Internally measured RX input power, channel 1 (LSB)	
36			Internally measured RX input power, channel 2 (MSB)	
37			Internally measured RX input power, channel 2 (LSB)	
38			Internally measured RX input power, channel 3 (MSB)	
39			Internally measured RX input power, channel 3 (LSB)	
40			Internally measured RX input power, channel 4 (MSB)	
41			Internally measured RX input power, channel 4 (LSB)	
42			Internally measured TX bias, channel 1 (MSB)	
43			Internally measured TX bias, channel 1 (LSB)	
44			Internally measured TX bias, channel 2 (MSB)	
45			Internally measured TX bias, channel 2 (LSB)	
46			Internally measured TX bias, channel 3 (MSB)	
47			Internally measured TX bias, channel 3 (LSB)	
48			Internally measured TX bias, channel 4 (MSB)	
49			Internally measured TX bias, channel 4 (LSB)	
50			Internally measured TX Power, channel 1 (MSB)	
51			Internally measured TX Power, channel 1 (LSB)	

52			Internally measured TX Power, channel 2 (MSB)	
53			Internally measured TX Power, channel 2 (LSB)	
54			Internally measured TX Power, channel 3 (MSB)	
55			Internally measured TX Power, channel 3 (LSB)	
56			Internally measured TX Power, channel 4 (MSB)	
57			Internally measured TX Power, channel 4 (LSB)	
58~65			Reserved channel monitor	
66~81			Vendor Specific	
82~85	4		Reserved	
86	12	Control	Tx Disable, channel 1~4	
87			Rx_Rate_select, channel 1~4	
88			Tx_Rate_select, channel 1~4	
89			Rx4_Application_Select, Rx Channel 4	
90			Rx3_Application_Select, Rx Channel 3	
91			Rx2_Application_Select, Rx Channel 2	
92			Rx1_Application_Select, Rx Channel 1	
93			Reserved/High Power Class Enable/Power set/Power override	
94			Tx4_Application_Select, Rx Channel 4	
95			Tx3_Application_Select, Rx Channel 3	
96			Tx2_Application_Select, Rx Channel 2	
97			Tx1_Application_Select, Rx Channel 1	
98	2		Tx/Rx_CDR_control, channel 1~4	FF
99			Reserved	
100	7	Free Side Device and Channel Masks	Masking Bit for TX/RX LOS indicator, channel 1~4	
101			Masking Bit for TX, Adaptive EQ fault indicator, channel 1~4 Masking Bit for TX Transmitter/Laser indicator, channel 1~4	
102			Masking Bit for TX/RX CDR Loss of Lock indicator, channel 1~4	
103			Masking Bit for Temperature alarm/warning	
104			Masking Bit for Vcc alarm/warning	
105~106			Vendor Specific	
107	12		Reserved	
108		Free Side Device Properties	Propagation Delay MSB	
109			Propagation Delay LSB	
110			Advanced Low Power Mode Far Side Managed Min Operating Voltage	
111~112			Assigned for use by PCI Express	
113			Free Side Device Properties	
114~118			Reserved	
119~122	4	Password Change	Password Change Entry Area	

		Entry Area		
123~126	4	Password Entry Area	Password Entry Area	
127	1	Page Select	Page Select Byte	

I2C Memory Map (A0 Upper Page 00h, Unlisted Fields are Blank / Empty)				
I2C Addr	**Size**	**Name**	**Description**	**Values (hex)**
128	1	Identifier	Identifier Type of serial Module(QSFP28)	11
129	1	Ext. Identifier	Extended Identifier of free side device. Includes power classes, CLEI codes, CDR capability	DC
130	1	Connector	Code for connector type(MPO_1x12)	0C
131~138	8	Specification compliance	Code for electronic compatibility or optical compatibility	
139	1	Encoding	Code for serial encoding algorithm	
140	1	BR, nominal	Nominal signaling rate, units of 100 MBd. For rate > 25.4 GBd, set this to FFh and use Byte 222	FF
141	1	Extended rateselect Compliance	Tags for extended rate select compliance	
142	1	Length(SMF)	Link length supported for SMF fiber in km (<1km)	01
143	1	Length(OM3) um)	Link length supported for EBW 50/125 um fiber (OM3), units of 2m	00
144	1	Length(OM2) um)	Link length supported for 50/125 um fiber (OM2), units of 1m	00
145	1	Length(OM1) 62.5 um)	Link length supported for 62.5/125 um fiber (OM1), units of 1m	00
146	1	Length(Copper) (Copper) (Copper)	Link length of copper or active cable, units of 1 m	00
147	1	Device tech	Device technology	
148~163	16	Vendor name	QSFP28 vendor name(ASCII)	
164	1	Extended Module	Extended Module codes for InfiniBand	
165~167	3	Vendor OUI	Free side device vendor IEEE company ID	
168~183	16	Vendor PN	Part number provided by free side device vendor(ASCII)	
184~185	2	Vendor rev	Revision level for part number provided by vendor(ASCII)	
186~187	2	Wavelength	Nominal laser wavelength (wavelength=value/20 in nm)	6658
188~189	2	Wavelength tolerance	The range of laser wavelength (+/- value) from nominal wavelength. (wavelength Tol. =value/200 in nm) or copper cable attenuation in dB at 7.0 GHz (Byte 188) and 12.9 GHz (Byte 189)	0BB8
190	1	Max case temp	Maximum case temperature	
191	1	CC_BASE	Check code for base ID fields (addresses 128-190)	
192	1	Link codes	Extended SpecificationCompliance Codes (See SFF-8024)	07

193~195	3	Options	Optional features implemented	
196~211	16	Vendor SN	Serial number provided by vendor (ASCII)	
212~219	8	Date Code	Vendor's manufacturing date code	
220	1	Diagnostic Monitoring Type	Indicates which type of diagnostic monitoring is implemented (if any) in the free side device. Bit 1,0 Reserved	
221	1	Enhanced Options	Indicates which optional enhanced features are implemented in the free side device.	
222	1	Baud Rate, nominal	Nominal baud rate per channel, units of 250 MBd. Complements Byte 140	
223	1	CC_EXT	Check code for the Extended ID Fields (addresses 192-222)	
224~255	32	Vendor Specific	Vendor Specific ID	

I2C Memory Map (A0 Upper Page 03h, Unlisted Fields are Blank / Empty)				
I2C Addr	**Size**	**Name**	**Description**	**Values (hex)**
128~129	2	Temp High Alarm	MSB at lower byte address	
130~131	2	Temp Low Alarm	MSB at lower byte address	
132~133	2	Temp High Warning	MSB at lower byte address	
134~135	2	Temp Low Warning	MSB at lower byte address	
136~143	8	Reserved		
144~145	2	Vcc High Alarm	MSB at lower byte address	
146~147	2	Vcc Low Alarm	MSB at lower byte address	
148~149	2	Vcc High Warning	MSB at lower byte address	
150~151	2	Vcc LowWarning	MSB at lower byte address	
152~159	8	Reserved		
160~175	16	Vendor Specific		
176~177	2	Rx Power High Alarm	MSB at lower byte address	
178~179	2	Rx Power Low Alarm	MSB at lower byte address	
180~181	2	Rx Power High Warning	MSB at lower byte address	
182~183	2	Rx Power Low Warning	MSB at lower byte address	
184~185	2	Tx Bias High Alarm	MSB at lower byte address	
186~187	2	Tx Bias Low Alarm	MSB at lower byte address	
188~189	2	Tx Bias High Warning	MSB at lower byte address	
190~191	2	Tx Bias Low Warning	MSB at lower byte address	
192~193	2	Tx Power High Alarm	MSB at lower byte address	
194~195	2	Tx Power Low Alarm	MSB at lower byte address	
196~197	2	Tx Power High Warning	MSB at lower byte address	
198~199	2	Tx Power Low Warning	MSB at lower byte address	
200~207	8	Reserved	Reserved thresholds for channel parameter set 4	
208~215	8	Reserved	Reserved thresholds for channel parameter set 4	
216~223	8	Vendor Specific		

224	1	Max TX&RX EQ		
225	1	RX out emphasis and amplitude		
226	1	Reserved		
227	1	FEC Control		
228	1	Maximum TC stabilization time		
229	1	Maximum CTLE settling time		
230	1	FEC ENABLE		
231	1	TX Squelch		
232	1	Reserved		
233	1	TX Freeze		
234~235	2	TX EQ		1
236~237	2	RX EQ		2
238~239	2	RX AM		3
240	1	TX&RX SQ		
241	1	RX OUT DISABLE&TX EQ CONTROL		
242~243	2	RX-PWR MASK	Masking bits for Rx input power alarms and warnings	
244~245	2	TX BIAS MASK	Masking bits for Tx bias alarms and warnings	
246~247	2	TX-PWR MASK	Masking bits for Tx output power alarms and warnings	
248~249	2	Reserved	Reserved channel monitor masks set 4	
250~251	2	Reserved	Reserved channel monitor masks set 5	
252~255	4	Reserved		

Tx Input Equalizer controls in upper page03 Byte234~235

Value	Transmitter Input Equalization	
	Nominal	Units
11xxb	Reserved	
1011b	Reserved	
1010b	10	dB
1001b	9	dB
1000b	8	dB
0111b	7	dB
0110b	6	dB
0101b	5	dB
0100b	4	dB
0011b	3	dB
0010b	2	dB
0001b	1	dB
0000b	0	NO EQ

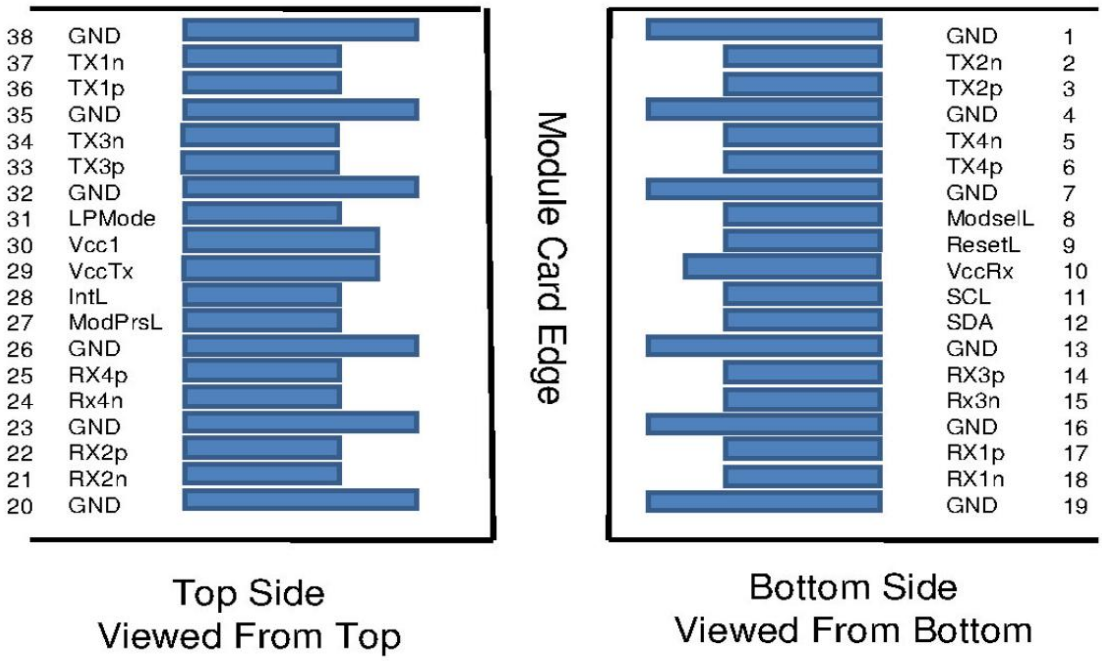
Rx Output Emphasis Controls in upper page03 Byte 236~237

	Receiver Output Emphasis At nominal Output Amplitude	
	Nominal	Units
1xxxb	Reserved	
0111b	7	dB
0110b	6	dB
0101b	5	dB
0100b	4	dB
0011b	3	dB
0010b	2	dB
0001b	1	dB
0000b	0	No Emphasis

Rx Output Differential Amplitude control in upper page03 Byte 238~239

	Receiver Output Amplitude No Output Equalization	
	Nominal	Units
1xxxb	Reserved	
0111b		
0110b		
0101b		
0100b		
0011b	600~1200	mV(p-p)
0010b	400~800	
0001b	300~600	
0000b	100~400	

PIN Assignmen



PIN Description			
PIN	**Symbol**	**Name/Description**	**Note**
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data output	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data output	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	+3.3V Power Supply Receiver	2
11	SCL	2-Wire Serial Interface Clock	
12	SDA	2-Wire Serial Interface Data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VccTx	+3.3 V Power Supply transmitter	2
30	Vcc1	+3.3 V Power Supply	2
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data output	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data output	

37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Notes

Notes1:GND is the symbol for signal and supply (power) common for the QSFP module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed . Recommended host board power supply filtering is shown in Figures 3 and 4. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ Module in any combination. The connector pins are each rated for a maximum current of 500 mA

ModSelL

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node must be biased to the “High” state in the module.In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met

ResetL

The ResetL pin must be pulled to Vcc in the QSFP module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module inidicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

ModPrsL

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted “Low” when inserted and deasserted “High” when the module is physically absent from the host connector

IntL

IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface.The IntL pin is an open collector output and must be pulled to host supply voltage on the host board.

LPMode

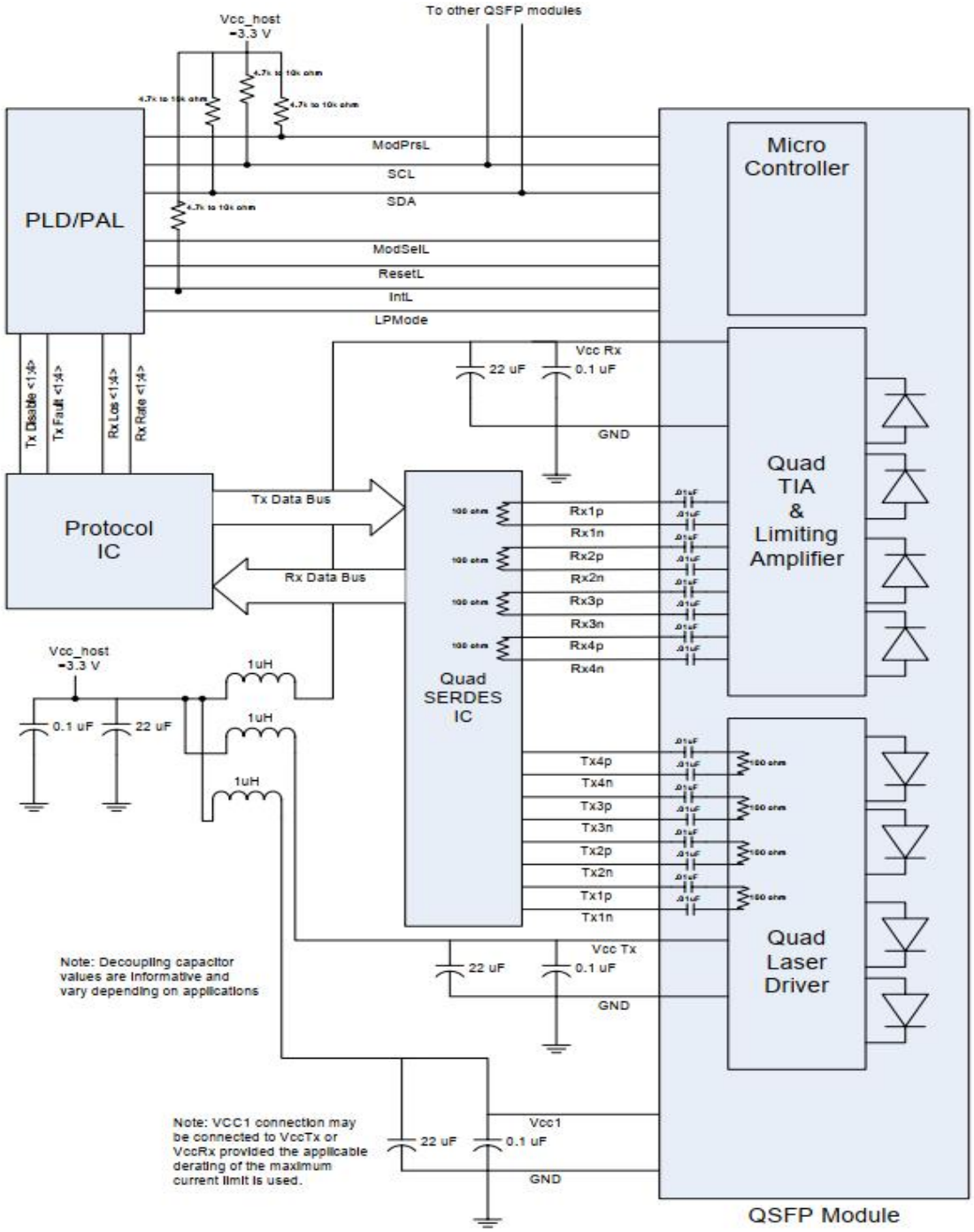
The LPMode pin shall be pulled up to Vcc in the QSFP module. This function is affected by the LPMode pin and the combination of the Power_over-ride and Power_set software control bits (Address A0h, byte 93 bits 0,1). The module has two modes a low power mode and a high power mode. The high power mode operates in one of the four power classes. When the module is in a low power mode it has a maximum power consumption of 1.5W. This protects hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

The modules 2-wire serial interface and all laser safety functions must be fully operational in this low power mode. The module shall still support the completion of reset interrupt in this low power mode. If the Extended Identifier bits (Page 00h, byte 129 bits 6-7) indicate a power consumption greater than 1.5W and the module is in low power mode it must reduce its power consumption to less than 1.5W while still maintaining the functionality above. The exact method of accomplishing low power is not specified, however it is likely that either the Tx or Rx or both will not be operational in this state. If the

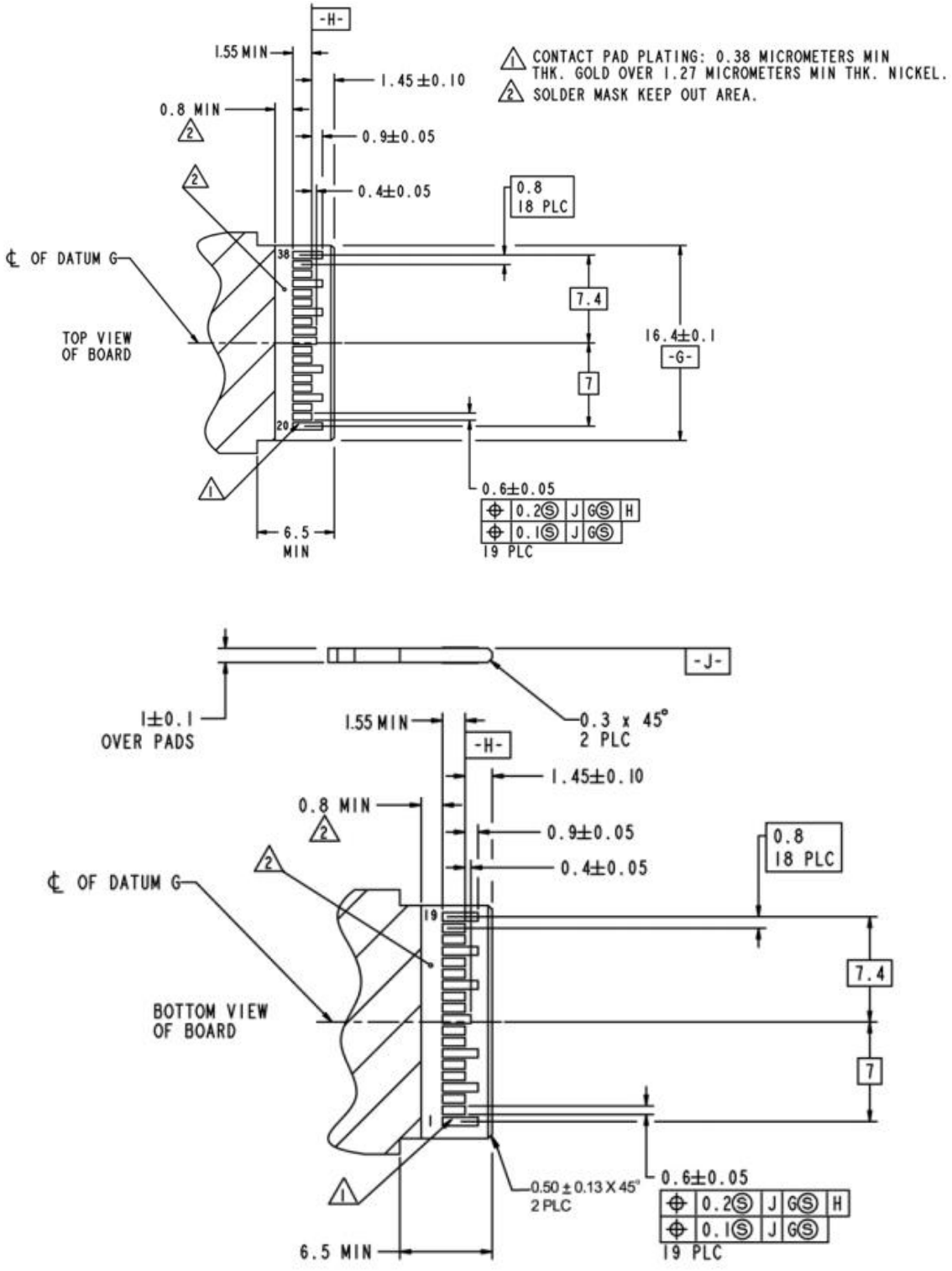
Extended Identifier bits (Page 00h, byte 129 bits 6-7) indicate that its power consumption is less than 1.5W then the module shall be fully functional independent of whether it is in low power or high power mode.

The Module should be in low power mode if the LPMode pin is in the high state, or if the Power_ over-ride bit is in the high state and the Power_set bit is also high. The module should be in high power mode if the LPMode pin is in the low state, or the Power_over-ride bit is high and the Power_set bit is low. Note that the default state for the Power_over-ride bit is low.

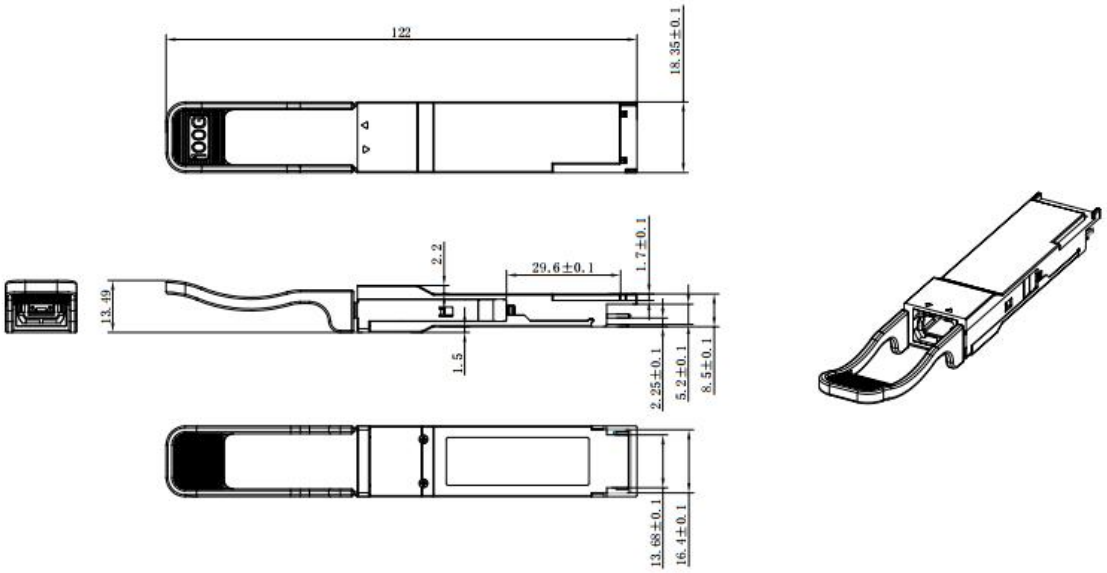
Electrical Interface



Recommended PCB Layout



Mechanical Dimensions



Notes:

1、Tolerance: +/-0.1mm.

2、Others according to SFF-8661 or customer spec .

3、Optical port according to fiber connector spec.

Warnings

Handling Precautions:

This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety：

Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.

Notice:

The information provided on this page contains the product target specifications which are subject to change without notice.

Check with your Litecore Sales Office for product updates, changes in specifications, sample availability and production release dates.